In the Specification

Amend the following numbered paragraphs of the specification:

[0005] A method and apparatus for testing large or very large scale integrated circuit packages is described. The testing equipment required for testing such packages is assumed to lack the number of channels necessary to connect one channel to each input/output of the unit under test. A computer program classifies all input terminals in a plurality of categories, each of which corresponds to a particular circuit type and electric network configuration connected to that pin. A unique set of DC levels is defined prior to testing for each class of inputs. These voltage levels are supplied by the tester channels, each of which drives a multitude of input pins that belong to the same category. The assignment of tester channels in the aforementioned arrangement is implemented by means of multiplexers that select for each pin the appropriate set of DC levels, and a memory buffer contained in the tester, with the DC test patterns stored wherein. The bit configuration of each pattern controls plural switching devices that deliver the appropriate DC levels to the terminals of the unit.

[0006] The practice of testing integrated circuit components is of prime importance to the electronic device manufacturer so as to weed out defective units before they are assembled and used. It is desirable to test semiconductor devices while they are still part of a wafer so as to discover unsatisfactory components prior to being mounted on the next level of packaging. Similarly, it is also desirable to test further these integrated circuit units after ~~that~~ they have been assembled on modules, cards or boards. Only by means of repetitive testing can the quality assurance of the devices be safeguarded. This continuous testing at each level of packaging imposes demands on the electronic industry to design and provide equipment that is capable of performing these tests in an automatic mode, at high speeds and with precise accuracy.

[0008] As integrated circuits become more sophisticated, the complexity of the supporting test equipment must increase correspondingly. This signifies a rapid increase of the number of tests that must be performed to locate all the faults in the integrated circuit. For example, on a simple integrated circuit of no more than a dozen circuits, at most, several tens of tests are sufficient to

locate all possible failures. In today's integrated circuits, ~~with its~~ containing hundreds and ~~soon~~ thousands of circuits, the number of tests required is in the order of many tens of thousands to achieve the same result. Not only the software requirements to generate such test patterns are difficult, but the time needed to apply them is inordinately long. A direct consequence of this trend toward miniaturization is that the test equipment must be able to process a large number of patterns at high speed. Such an electronic tester is usually controlled by a computer. The tester generates a signal that is provided to the integrated circuit or assembly, hereinafter referred to interchangeably as a unit under test (UUT). This signal which is in the form of a forced voltage or current is supplied to the appropriate input terminal pin by an electronic network called "digital-to-analog converter" or "D/A converter"~~, ain short~~. This, and other pertinent circuitry forms a "tester channel". As the name ~~states it~~ suggests, it converts a "logic binary level" into an electrical analog level which is applied to a single input terminal of the unit under test (UUT). In a similar fashion, the actual electrical response at the output pins of the UUT is compared to a standard acceptable response by the computer. These responses are dictated by the test patterns. For example, if the expected binary level at one output pin of the UUT is a "logic 1", the tester, by use of the channel connected to that output pin, will measure the voltage or current level. A nonconcurrence between the measured and expected levels indicates the presence of a failure inside of the integrated circuit, and the unit is discarded as defective.

[0012] In effect, this invention provides an advance over the prior art by enabling a tester with ~~much less~~ fewer channels than those required by the integrated circuit package to actually test this package as if an adequate number of channels were available. This invention provides that tester channels can be multiplexed to "banked" sets of terminal pins containing with input receivers and/or output drivers without requiring that the banked sets of terminal pins share a common circuit type and electric network configuration. In particular, this invention is useful to test large scale integrated packages that represent the latest advances in technology with existing test equipment whose architecture and characteristics have not fully matched the advances in semiconductor technology packages.

[0016] The ASIC boundary scan design supports reduced pin testing in a fashion similar to IEEE

Standard 1149.1, published in 1990 by the IEEE Standard Test Access Port and Boundary Scan Architecture. In ASIC boundary scan design the scan chains have a dedicated test access port which separates the device test into two testable regions. The region internal to the boundary scan chain consists of all the logic circuitry, embedded memory, and cores. This internal region can be fully tested using a reduced number of test pins consisting of test control inputs, scan chain I/O, and test I/O. The region external to the boundary scan chain contains the same internal test controls and I/O. It also includes all the external I/O pins. These are all the remaining functional and data I/O on the product.

[0021] The Automatic Test Pattern Generator (ATPG) for the External I/O tests targets special parametric faults: faults to specifically test off-chip drivers and receivers. The ATPG tool also segregates the external logic (that connected to the External I/O plus the necessary test control logic). By targeting only the parametric faults and using only the external logic, the ATPG patterns are very structured and very simple, either applying tester stimulus to the External inputs pins, and observing them in the boundary latches, or ~~else measure~~ measuring the output of the External drivers after applying the driver enable and data signals from the boundary scan latches.

[0023] The present invention involves a method known as "banking," which ~~is a method that~~ switches a predefined group of tester channels between "active" (connected) and "inactive" (unconnected) groups of pins on ~~the product~~ an integrated circuit and allocates groups of I/O pins to specific tester channels. One banking technique is to implement it directly on a module test fixture, which mates the integrated circuit to the tester. As an example, as shown in Fig. 2, a module test fixture with banking can extend a tester with 512 tester channels to test a product with 1,592 test pins. To begin, 150 tester channels could be fixed to always contact 150 of the product's pins to handle the RPCT test I/O. Configuring the banking can use a 1:4 multiplexer. Two tester channels are needed to control the banking multiplexer on the module test fixture. The remaining 360 tester channels can be switched between four banked groups. Each banked group, when active, would connect to 360 external I/O pins on the product. The 1:4 multiplexed banking extends the 360 tester channels to support testing of 1,440 products pins. Therefore, the 150 fixed channels plus the 360 channels banked to four groups extends the 512 pin tester to test products with up to 1,590 pins.

[0029] The present invention enables testing of new high pin count products on existing testers with fewer test pins. This invention works with all types of I/Os standards, including differential I/O and I/O requiring reference voltages. There is no loss of parametric fault coverage, allowing high quality test while avoiding the capital and production costs associated with purchasing and operating a ~~new~~ high pin count testers.

[0032] The cost of Automatic Test Equipment (ATE) has a direct relationship to the number of test channels on the tester. Presently, when products have pin counts and volumes that exceed the capacity of existing testers, expensive ~~new~~ higher pin count testers must be purchased. Future technology offerings will lead to products with even higher pin counts. Banking External I/O test patterns can avoid the purchase of these new testers by allowing such products to be tested on existing lower pin count testers.

[0033] Automatic Test Pattern Generation (ATPG) can be used to bank the External I/O test patterns such that they can be applied on the low pin count testers using a banked module test fixture. The ATPG of External I/O test patterns for earlier banking methods assumed that ~~at most~~ just only one external I/O pin could receive a stimulus during execution of a test pattern. For every external I/O pin, the three receiver parametric tests of logic 1 and 0 were each generated as a separate test pattern. The driver parametric test patterns were allowed to measure any number of pins. Manufacturing test could then organize the receiver tests into the banked pattern sets conforming to the banked pin groups defined by the module test fixture. The receiver tests were banked into pattern sets, each containing the tests for the pins in a banked group. The driver tests were included in all the grouped pattern sets. ~~Measures~~ Voltage measurements during ~~within~~ the driver tests were ignored when the measured pin was not active in a particular group. Since every External I/O pin was active in at least one group, every pin's receiver and driver tests are applied by one of the banked pattern groups. The complete independence of the external I/O pins and their test patterns also allowed banked module test fixtures to be shared by products with the same physical size and image.

[0035] ATPG tools do not support importing information about the physical location of the chip

I/O's and their module pin mapping. Test generation uses a logical model of a chip and its I/O. The actual physical location of these I/O on the chip is defined separately by the physical design process. In addition, the secondary mapping of the chip I/O to module pins is defined by yet another process~~. The~~, the design of the module substrate. In some cases, the same product can be packaged on different module substrates.

[0038] As manufacturing ~~gets~~ receives future orders for high pin count and high volume products, the continued economic interest is to minimize capital costs and production costs by testing the product on existing testers or less expensive testers with fewer tester channels ~~then~~ than the product has pins.~~:~~ Because of the special I/O pins described above, a customer's test generation for the external I/O tests will continue to be run to with the assumption that the tester will contact all the product pins simultaneously. However, after receiving the test patterns, manufacturing can use a new banking method to modify the external I/O test patterns such that they can be applied on testers with fewer test channels using custom banked test fixtures or an intermediate banking board.

[0039] The banking method used in the present invention handles the ~~measures~~ measurements performed during ~~within~~ the external I/O driver tests in the same fashion as the earlier method. However, by utilizing re-simulation of the suitably modified external I/O test patterns, this method does not restrict the tests to just one stimulus per test pattern on the external I/O pins. Any and all of the pins in the active bank can have stimuli applied by one of the re-simulated test patterns. Since the designer's test generation is done assuming all pins will be contacted then there are many fewer test patterns each containing stimuli on many external I/O pins. Consequently, even after replication of the external I/O test patterns for each bank, the net result is that the modified and re-simulated external I/O test patterns are far fewer in number and will require less time to apply in comparison to the earlier banking methods.

[0044] b. In each external test mode, the driver data signal must be controllable (to 0 and 1) from a scannable latch or test input. The latch is called a driver boundary latch. Intervening logic that ~~is sensitizable~~ can be sensitized to an active state is allowed.

[0045] c. In each external test mode, the driver enable signal must be controllable (to 0 and 1) from a scannable latch, or test input or must be physcially tied enabled (1). The latch is called an enable boundary latch. Intervening logic that ~~is sensitizable~~ can be sensitized to an active state is allowed.

[0048] f. There must exist a static sensitizing state, which may include test inputs and/or scannable latches, for which rules a, b and c are simultaneously satisfied for all non-tested I/O.

[0050] 3. For typical external I/O pins in the parametric test patterns, the ASIC Boundary Scan Design Rules cause the preconditioning of each parametric fault objective on typical external I/O pins to be entirely independent of the preconditioning for other parametric fault objectives. When one test pattern contains the tests of many parametric faults, the preconditioning and test of individual parametric faults can be separated from that original test pattern and regrouped into two or more "banked" test patterns. Thereby, each full pin count test pattern can be separated into "banked" test patterns.

[0051] 4. The future introductions of other types of external I/O with special interdependencies are highly unlikely to compromise this banking test methodology. This method allows all pins that are continuously contacted plus all pins in a given bank to have stimuli and ~~measures~~ measurements within the same test pattern. In order to compromise this methodology, the number of external I/O on a product with such an interdependency would have to exceed the number of pins in the union of the group of continuously contacted pins and a "banked" group of pins.

[0054] 7. ASIC Boundary Scan Design Rules allow the customer's external I/O test patterns to be modified and re-simulated into banked test patterns without need to repeat either test generation or fault machine simulation. The structural nature of the ASIC Boundary Scan Design requires only good machine simulation (GMS) after the full pin count test patterns and their parametric preconditioning has been separated into "banked" test patterns.

[0057] The designer will continue to design the product, run test generation, and submit the external I/O test patterns without knowledge of the banking configuration that will later be determined by manufacturing. Each test in the test patterns may contain any number of stimuli ~~and~~

~~measures~~ measurements producing a corresponding output on the external I/O pins. As provided by the customer, the external I/O test patterns obtain high parametric fault coverage and require a full pin count tester.

[0058] Attention is directed to Figure 1 which shows the process steps used in the present invention. The first process described below analyzes an ASIC product's physical design data, logical test data, and module description. It recognizes the presence of differential I/O, voltage reference I/O and any other types of I/O that have special banking restrictions. The banking constraints required for these exceptional types of I/O pins is defined to the process by a set of rules. Rules can also be included which define guidelines that allow design and build optimization and reuse of module test fixtures or the programming of the channel assignments within the intermediate banking box. For a high pin count ASIC, this process generates a list of allowable banking configurations for the product. Multiple "banking" configurations are possible for each ASIC. With this flexibility, two or more ASIC products can be "banked" in the same configuration. The most general "banked" configuration for ASICs with a common physical image can be used allowing multiple products to share the banking configuration and hardware.

[0063] Refer to a table of existing module test fixtures to identify ~~opportunies~~ opportunities for reuse and guidelines that address design optimization for new or modified module test fixtures.

[0070] ~~Replace~~ Reset all the Measure Latch Events for which a voltage measurement is obtained with Dummy Measured Latch Events prior to resimulation; and

[0071] ~~Replace~~ Reset all the Primary Output ~~Measures~~ Measurements with a ~~Measure~~ "Measurement Unknown" prior to re-simulation of the primary output.

[0073] The GMS re-establishes ~~measures~~ measurements in each "banked" copy of the test patterns.

[0074] These new ~~measures~~ measurements are no longer dependent on any Stimuli on pins in an "inactive" bank.

[0076] Remove all Primary Output ~~Measures~~ Measurements on "inactive" (out-of-bank) pins.

[0077] Every Primary Output ~~Measure~~ Measurement in the original pattern set will be retained in at least one of the "banked" pattern sets. The "banked" copies of the test patterns also contain preconditioning from the Stim Latch Events. The preconditioning from these Stim Latch Events is for the "driver" tests of all the External I/O pins. After the GMS, each of the "banked" copies of the test patterns will contain "driver" test ~~measures~~ measurements on all the External I/O pins. Each "banked" copy will have these ~~measures~~ measurements on both its "active" (in-bank) and "inactive" (out-of-bank) pins. Within these "banked" copies, those ~~measures~~ measurements on the "inactive" (out-of-bank) pins are removed. In one "banked" copy of the test patterns, they are guaranteed to be "active" (in-bank) and thus remain as active ~~measures~~ measurements. Each ~~measure~~ measurement need only be done once to preserve the parametric fault coverage of the original pattern set.

[0078] 5) Remove any tests that contain no ~~measures~~ measurements on latches or ~~POs~~ Primary Outputs after being grouped and resimulated

[0080] The Sum of the Parts. ~~-~~